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The communication system for advanced automotive control applications

FlexRay International Workshop

4th March 2003

Detroit

FlexRay - The electrical physical layer

Bernd Elend - Philips Semiconductors



FlexRay - The electrical physical layer

- Network topology
 - Cable termination
 - ECU architecture
 - Bus driver
 - Power modes & wake up
 - Bus guardian
-
- Status of development
 - Outlook to future products

Electrical
Physical
Layer
Specification

Philips products

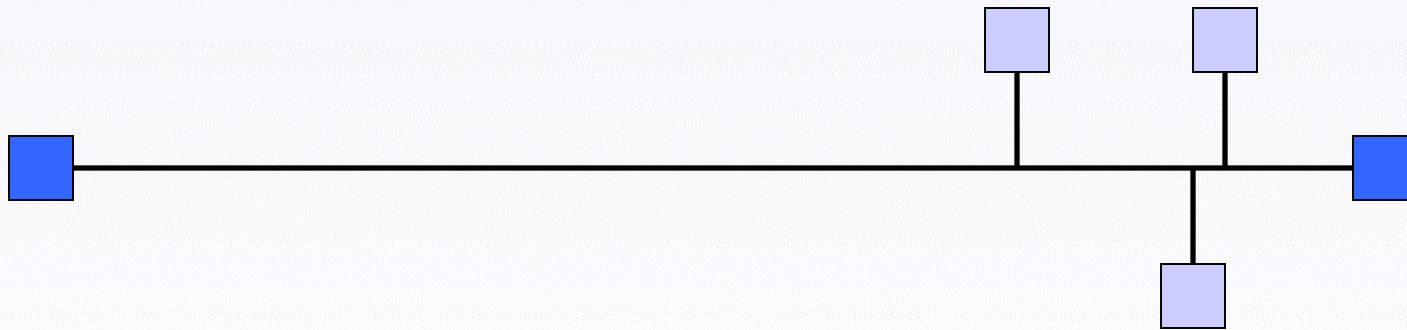
FlexRay - The electrical physical layer

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Network topology - requirements

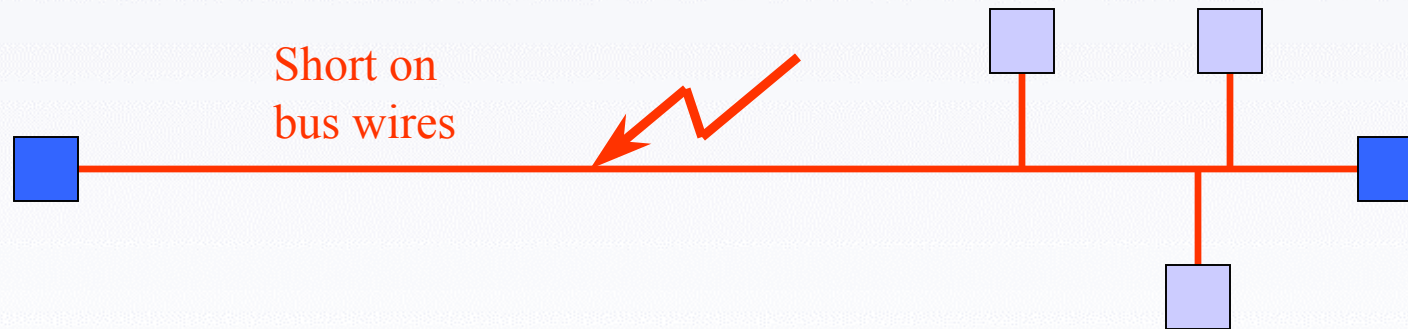
- Main requirements of a FlexRay network topology:
 - Containment of failures in network sections
 - Support for redundant channels
 - Flexible and extensible layout

Network topology – passive bus



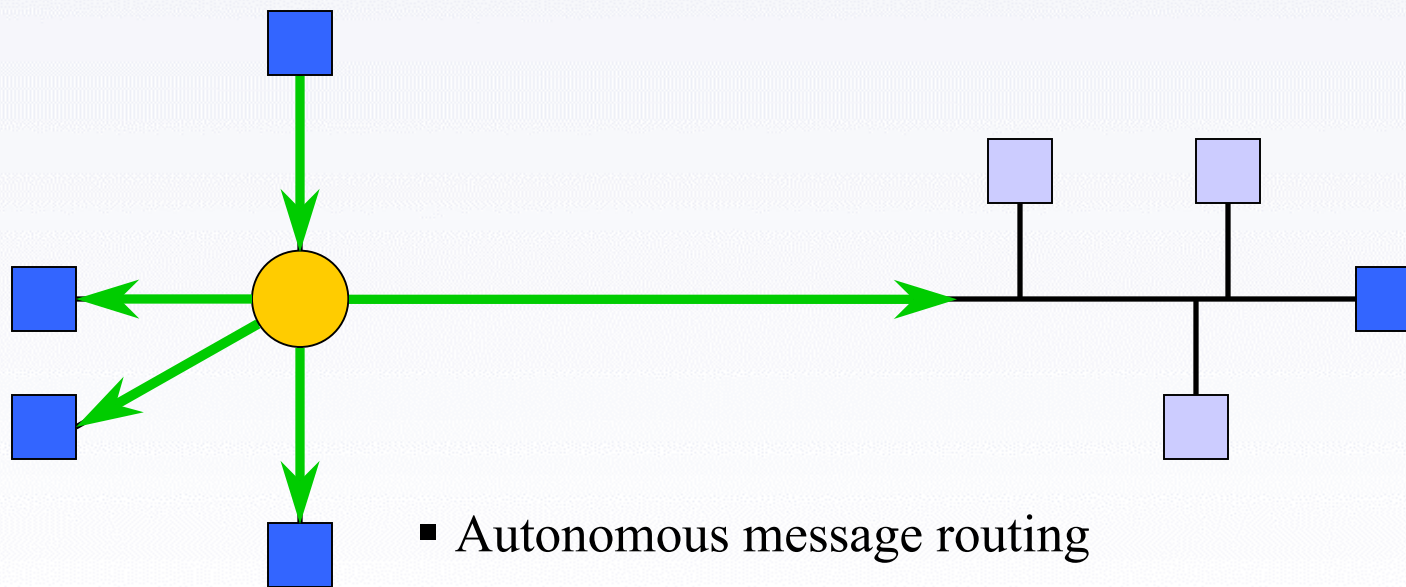
- Maximum 8 stubs in a 10 Mbit/s network
- Maximum 0.2 m length of stub
- Maximum 12 m cable length between nodes
- Acceptable EMC performance achievable

Network topology – passive bus



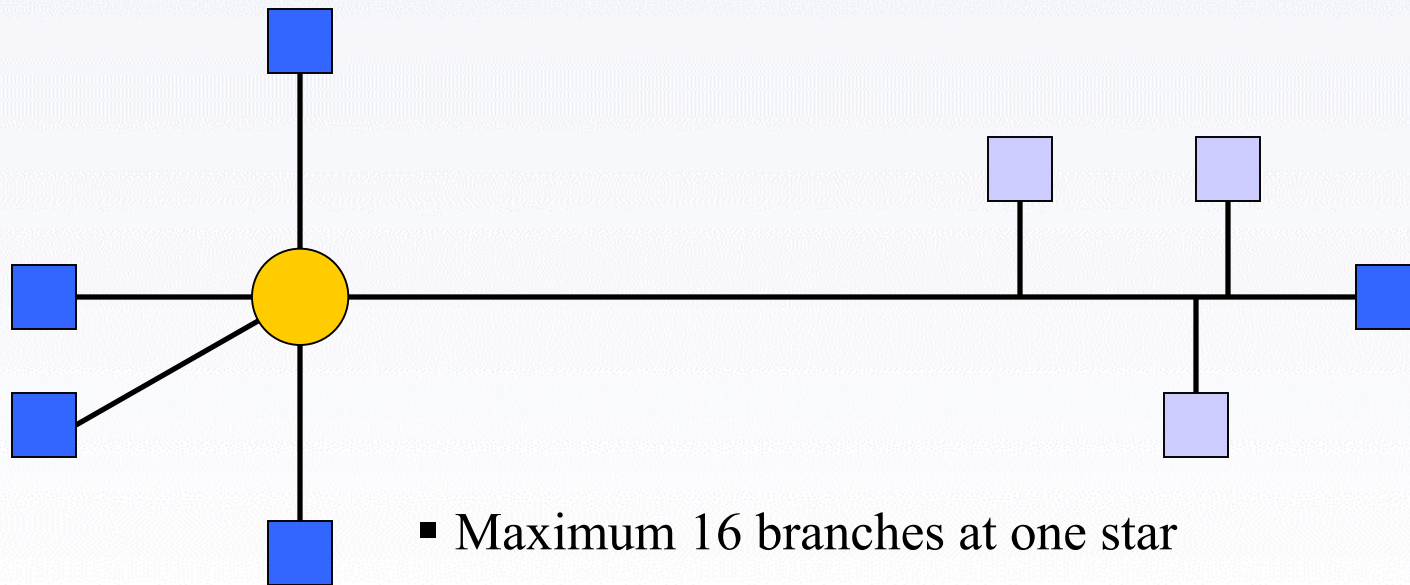
- Maximum 8 stubs in a 10 Mbit/s network
- Maximum 0.2 m length of stub
- Maximum 12 m cable length between nodes
- Acceptable EMC performance achievable
- All in all feasible, **but NO fault containment**

Network topology – active star



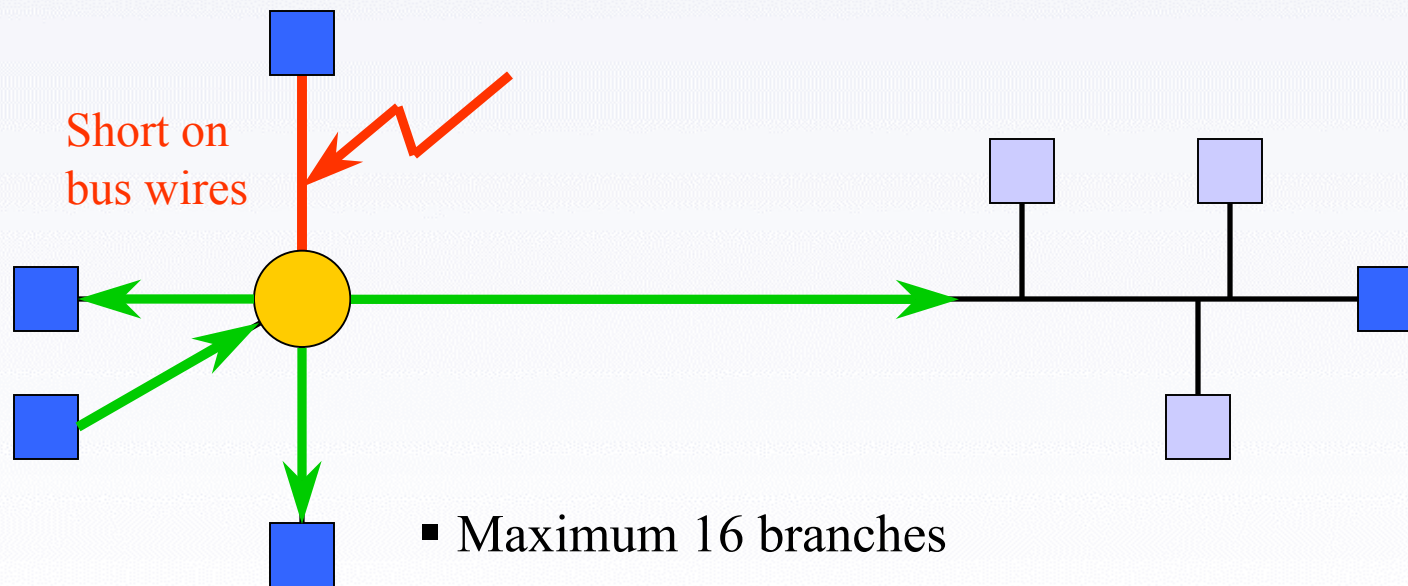
- Autonomous message routing
- Autonomous power management
(*wake-up and go to sleep*)

Network topology – active star



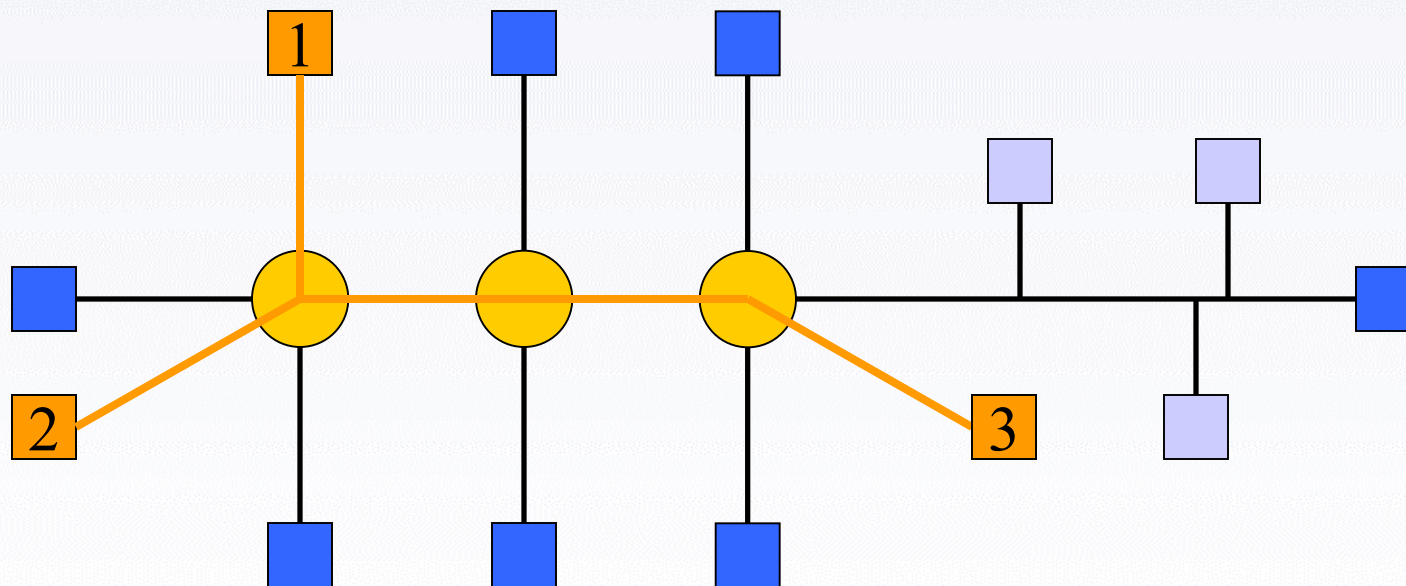
- Maximum 16 branches at one star
- Maximum 24 m length of branch (without stubs)
- Maximum 12 m length of branch (with stubs)
- Improved EMC performance

Network topology – active star



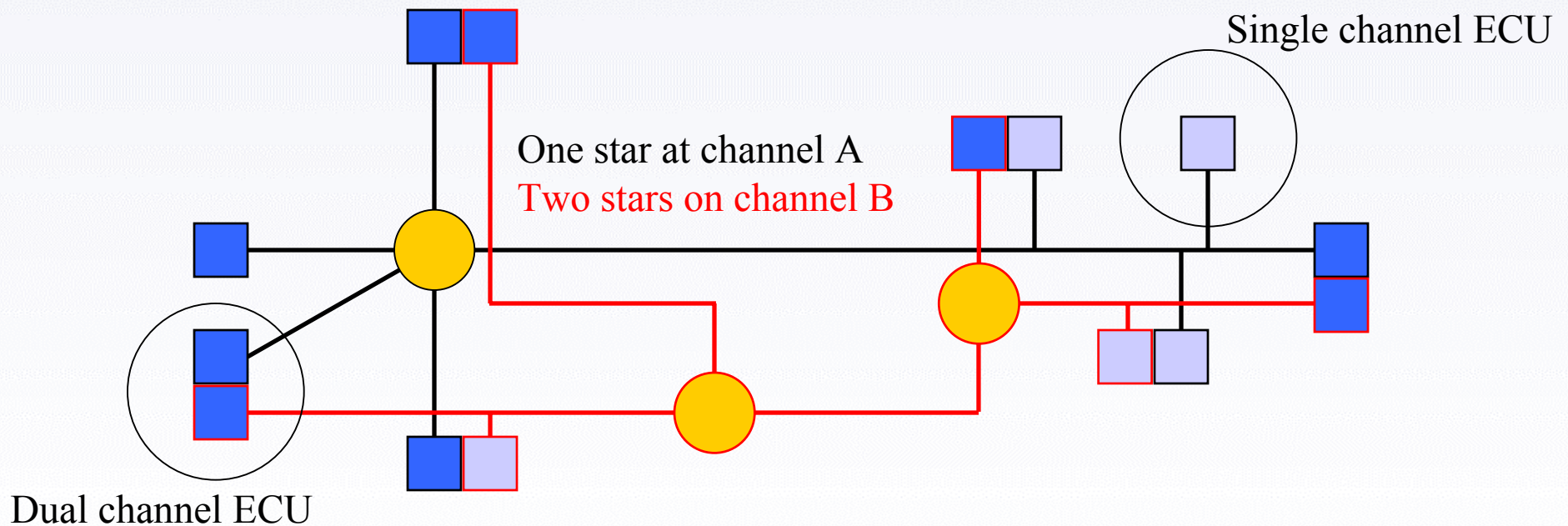
- Maximum 16 branches
- Maximum 24 m length of branch (without stubs)
- Maximum 12 m length of branch (with stubs)
- Improved EMC performance
- **Fault containment on branches**

Network topology – cascaded active stars



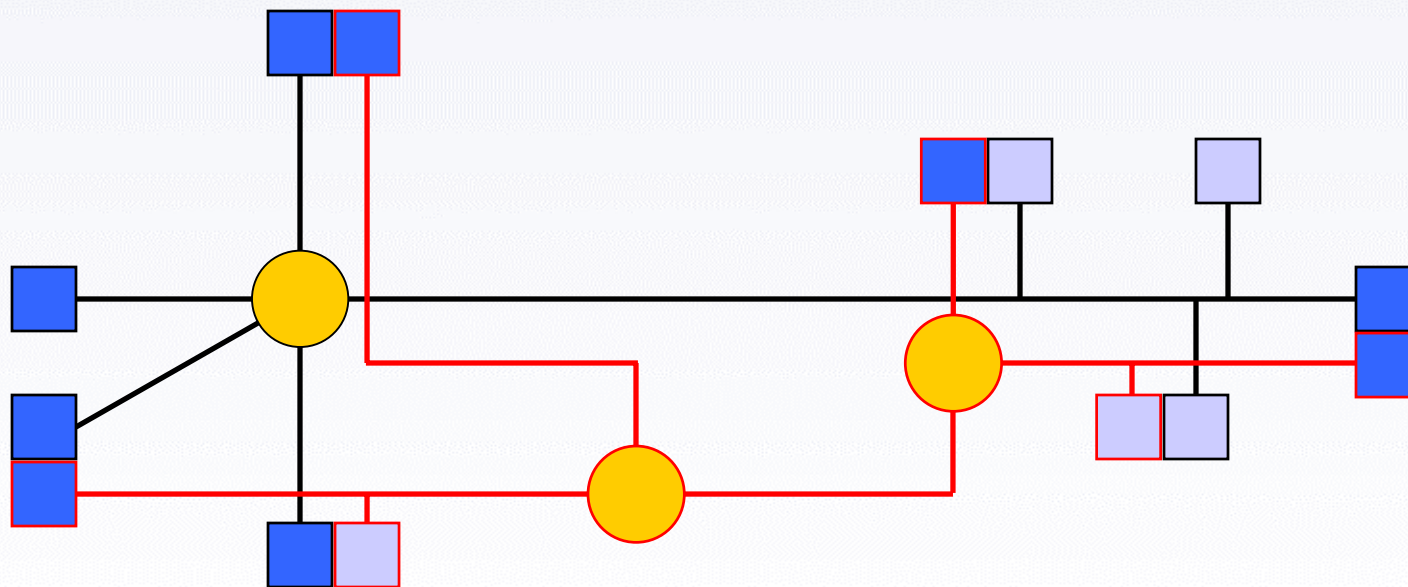
- Maximum 3 cascaded stars
- Different propagation delays are handled by the clock synchronization algorithm without prior knowledge

Network topology – dual channel



- Possibilities within a dual channel network
 - Different channel layouts
 - Mix of dual and single channel nodes

Network topology – dual channel



- Protocol supports use of dual channel network for ...
 - ... redundancy
 - ... doubled bandwidth

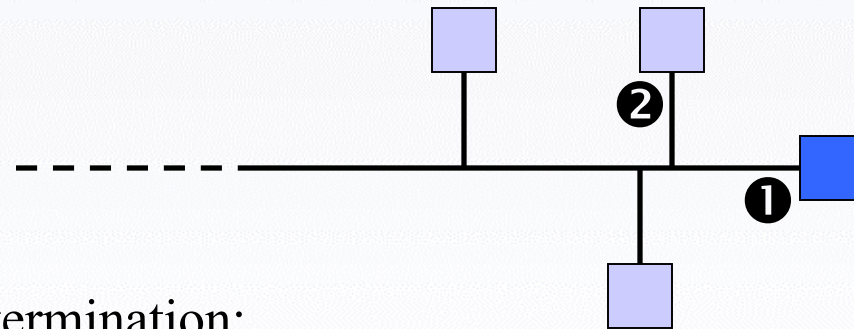
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Network topology – cable termination

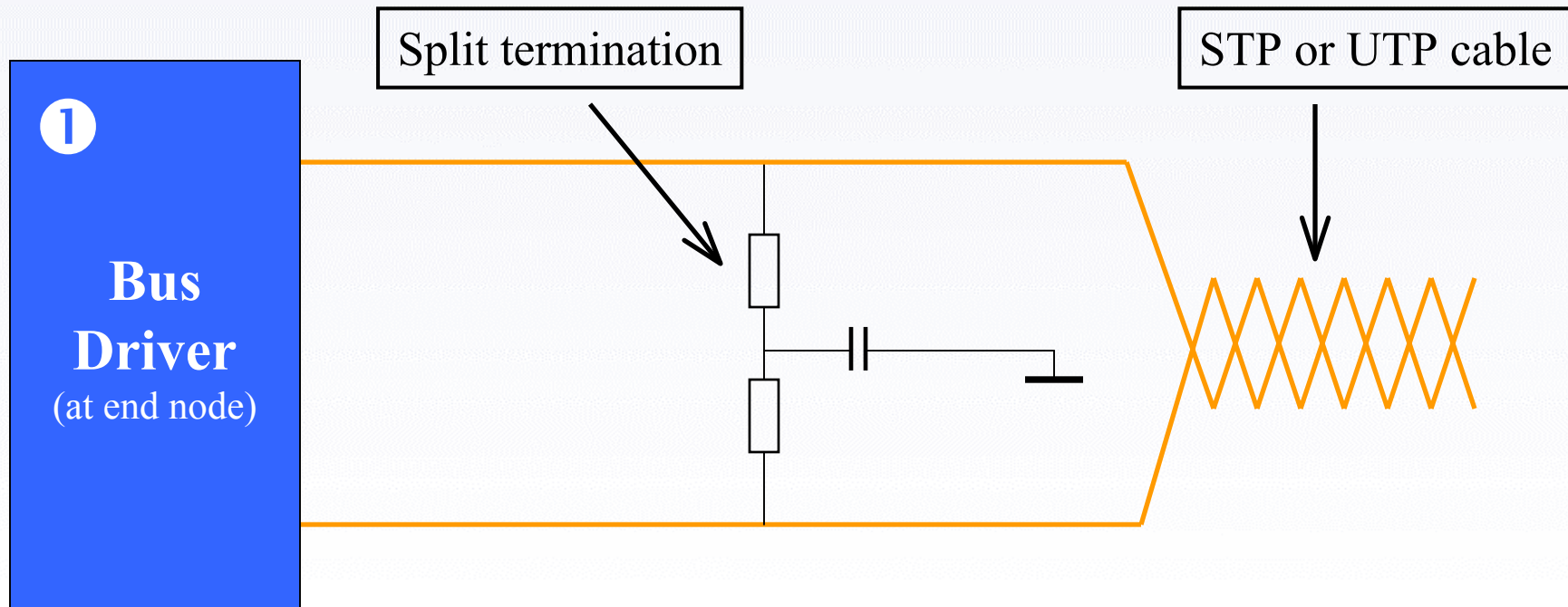
- Main requirements for the cable termination:

- Guarantee predefined bus levels
- Prevent reflections

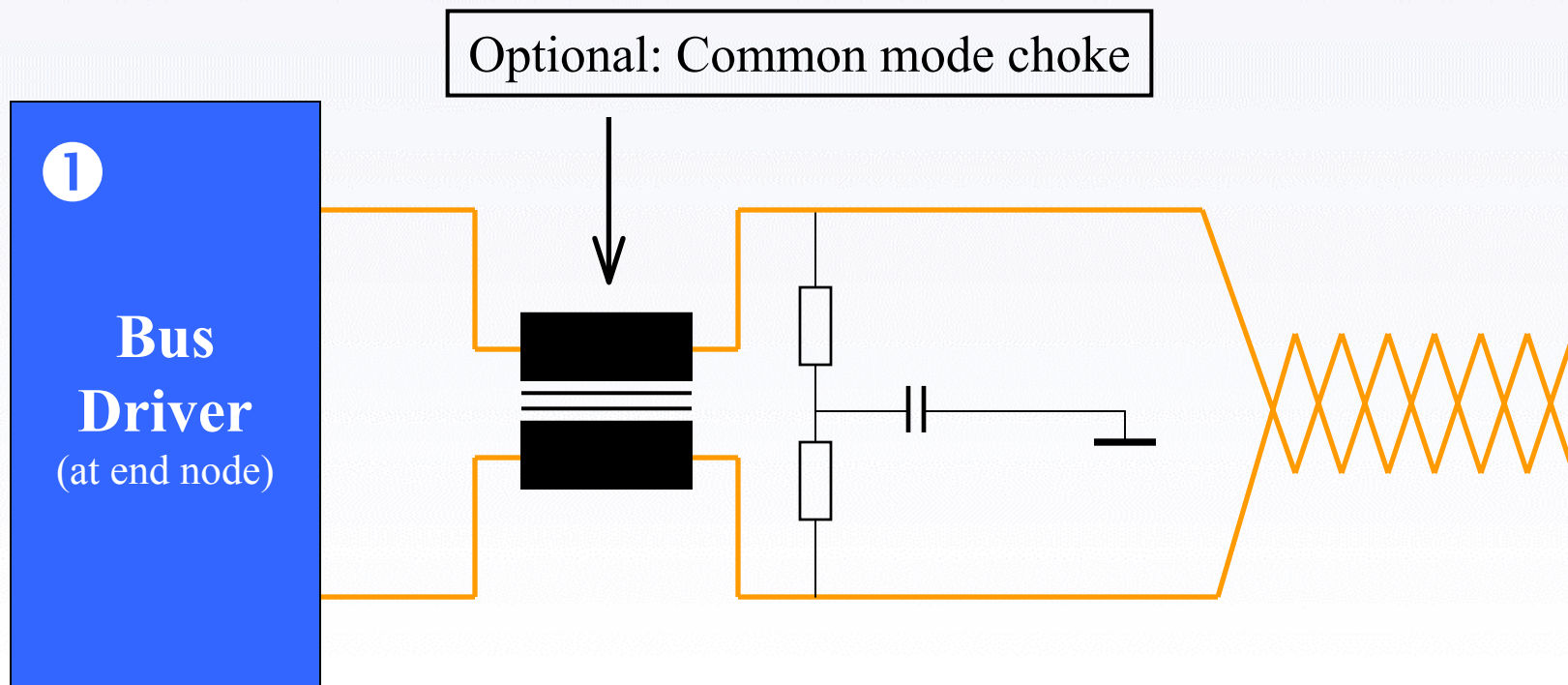


- Different types of termination:
 - ① End nodes (and stars)
 - ② Stub nodes

Network topology – cable termination

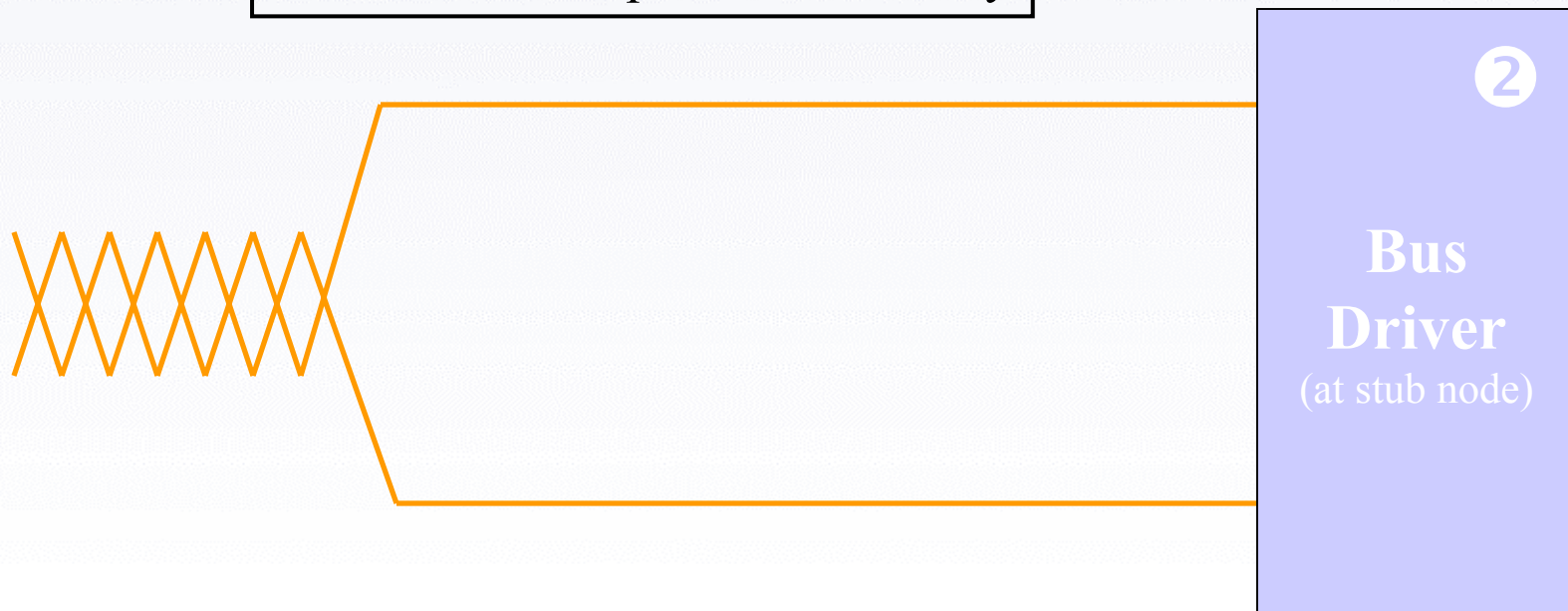


Network topology – cable termination

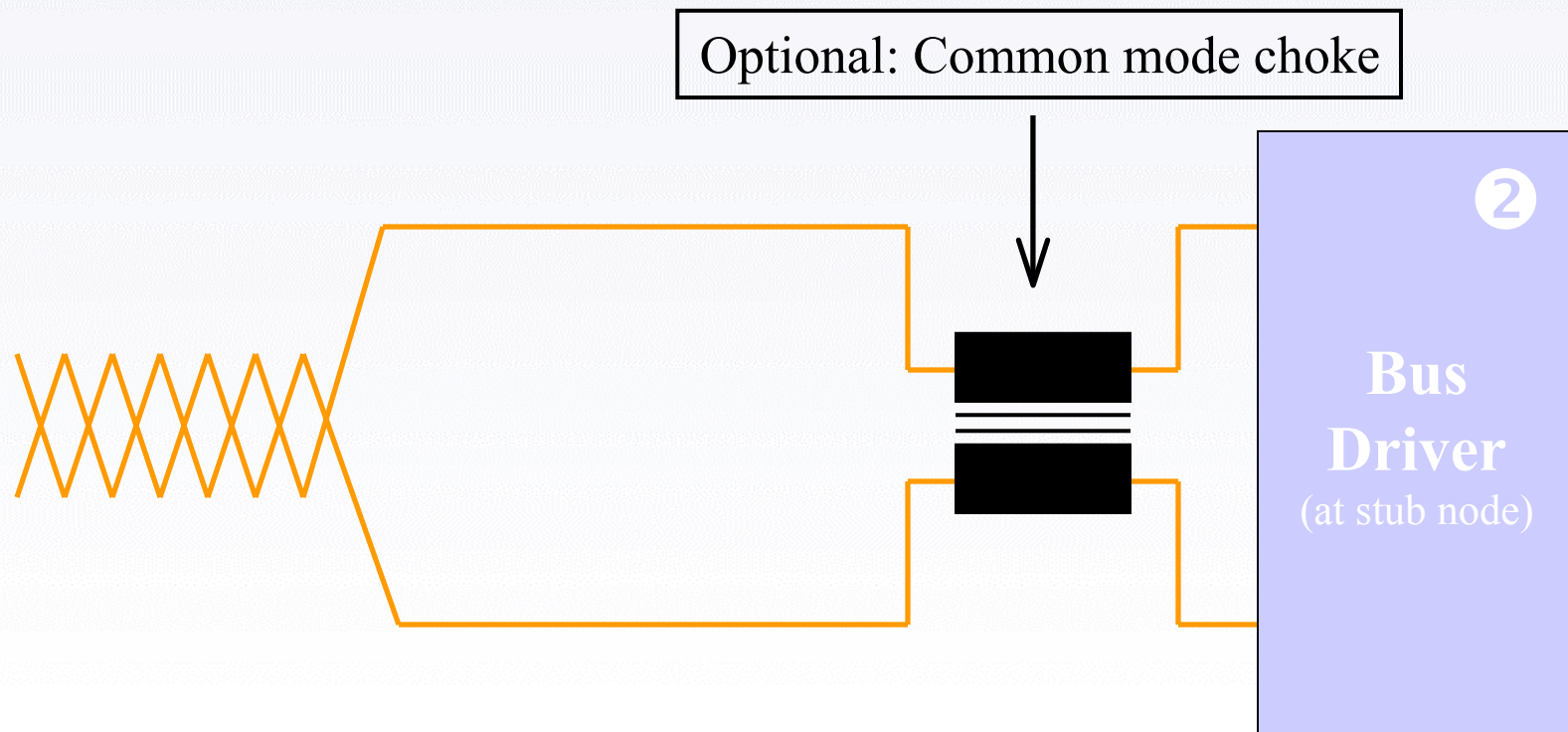


Network topology – cable termination

No external components necessary



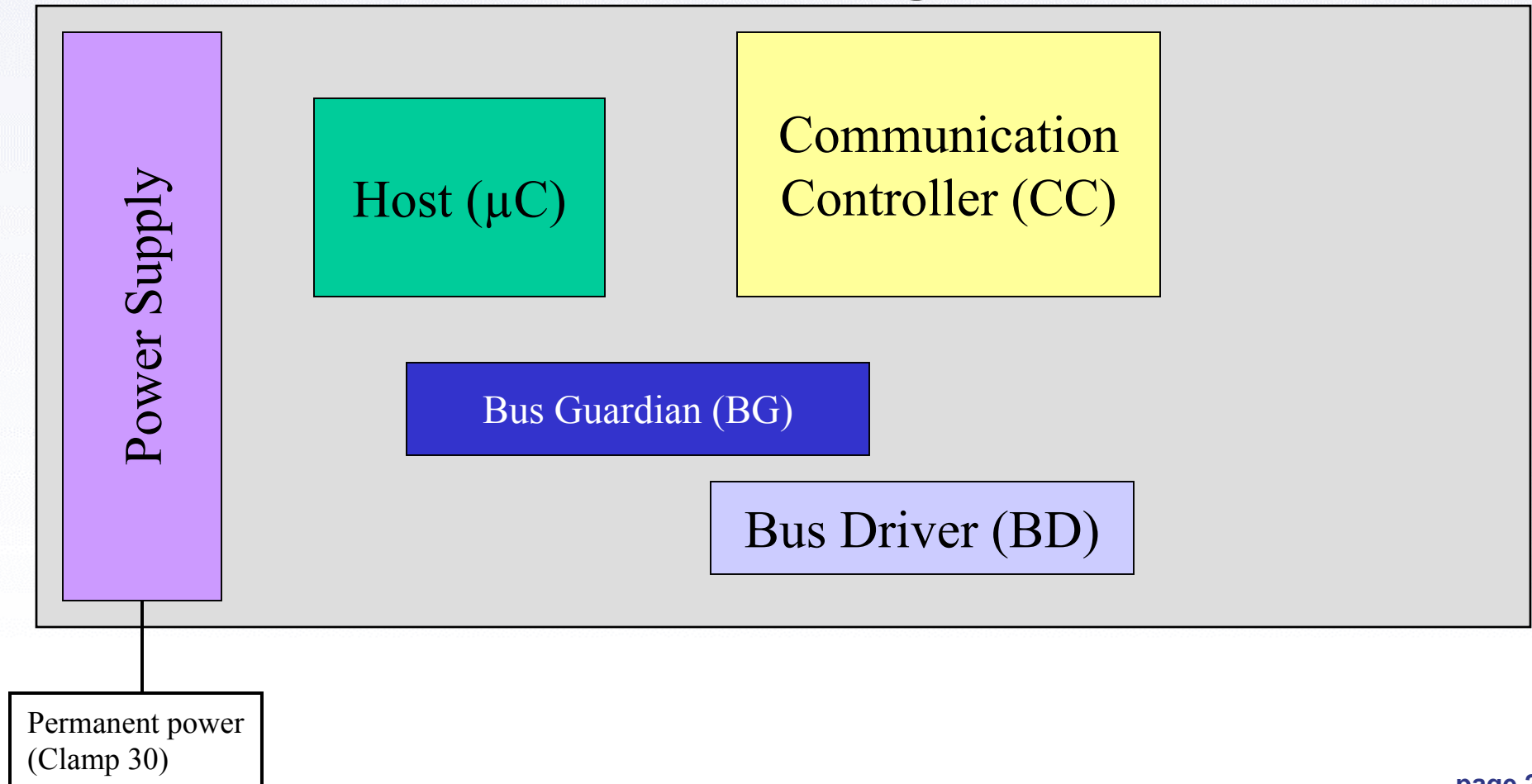
Network topology – cable termination



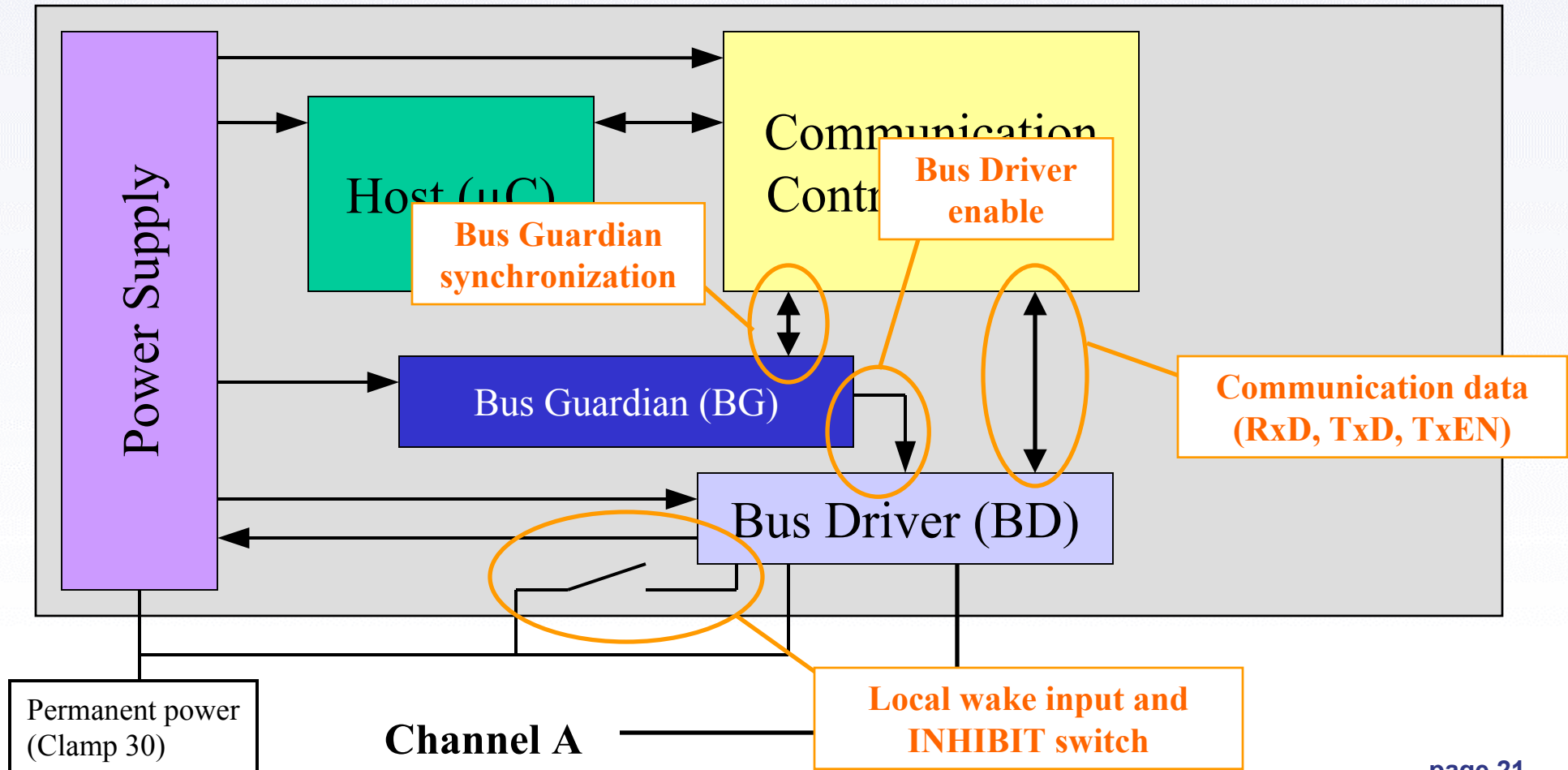
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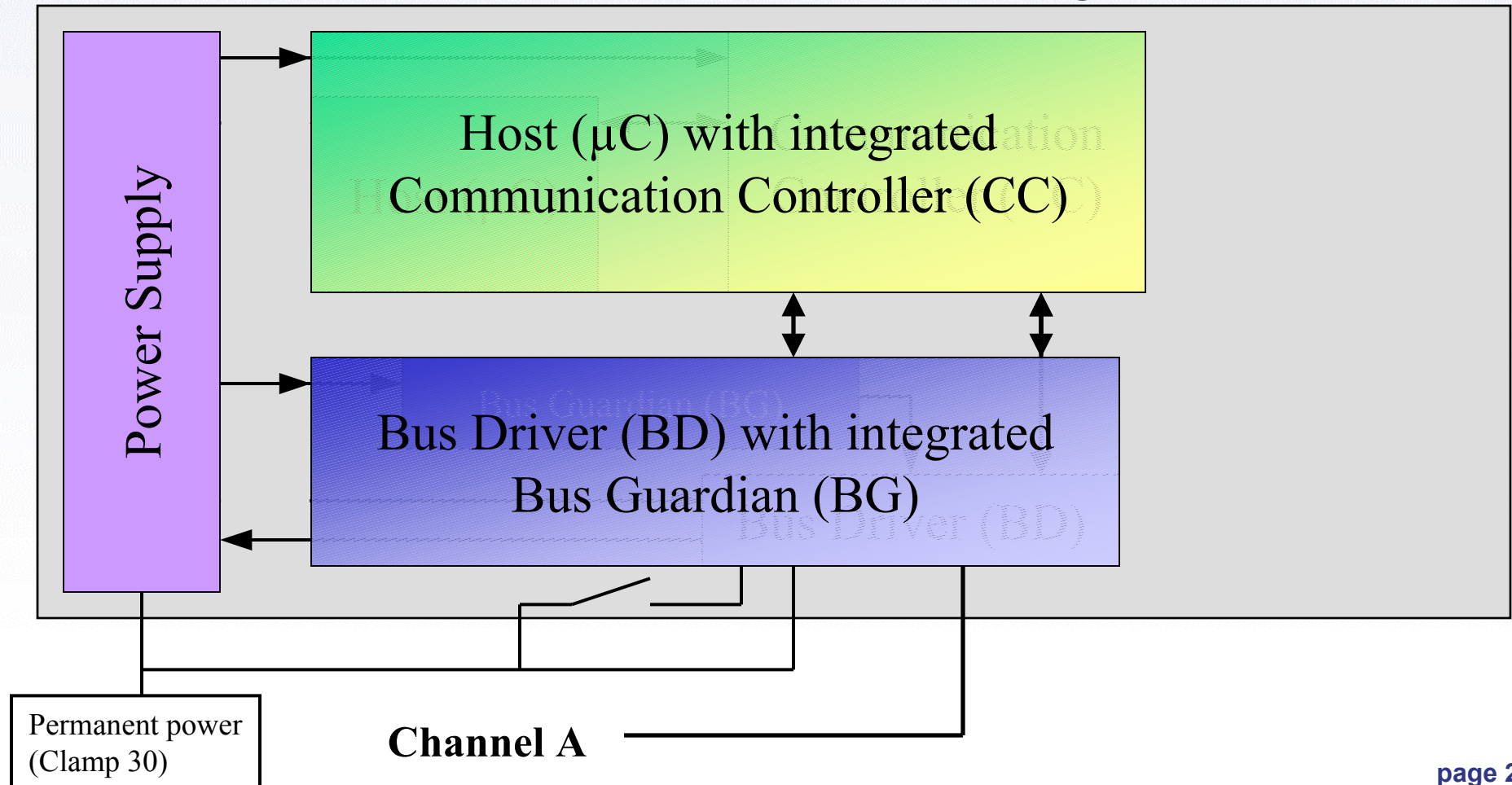
ECU architecture - single channel ECU



ECU architecture – main interfaces



ECU architecture – future layout

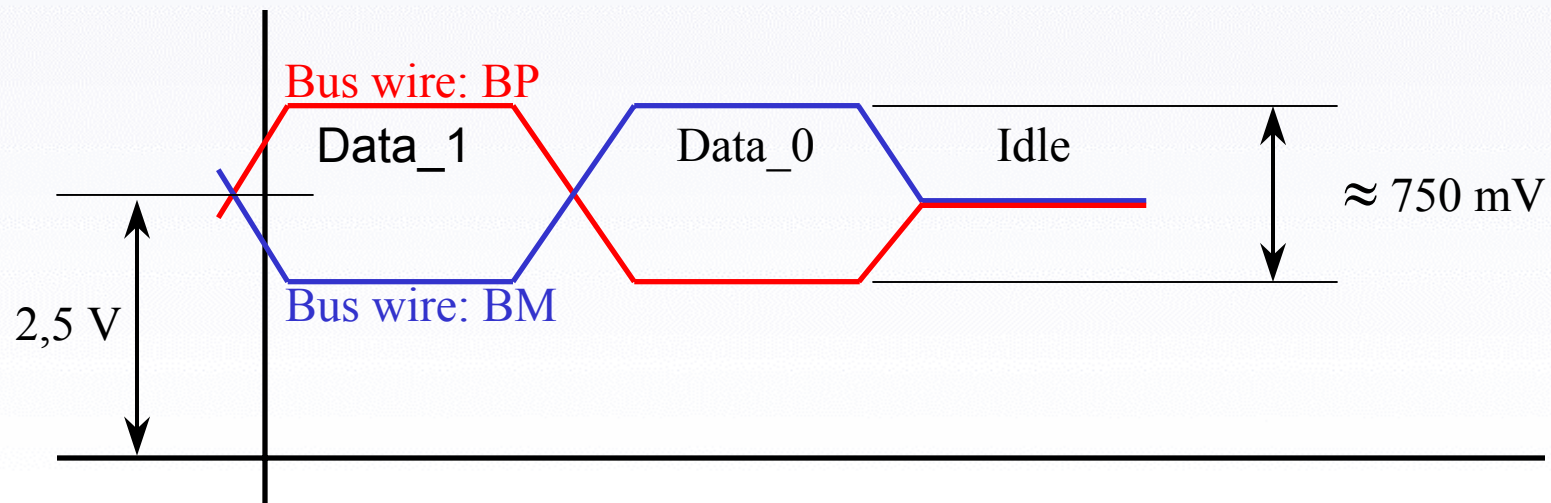


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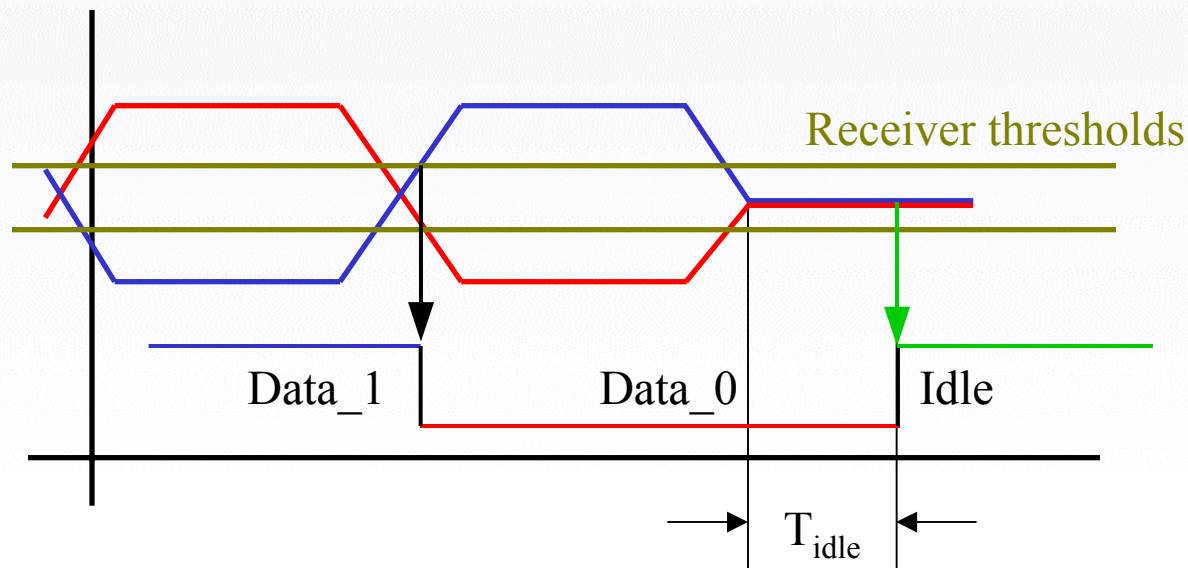
Bus driver – bus level scheme

- Transmitter properties:
 - Both signal states are dominant
 - Only idle is recessive



Bus driver – bus level scheme

- Receiver properties:
 - Thresholds symmetrically to Idle level
 - Wide hysteresis

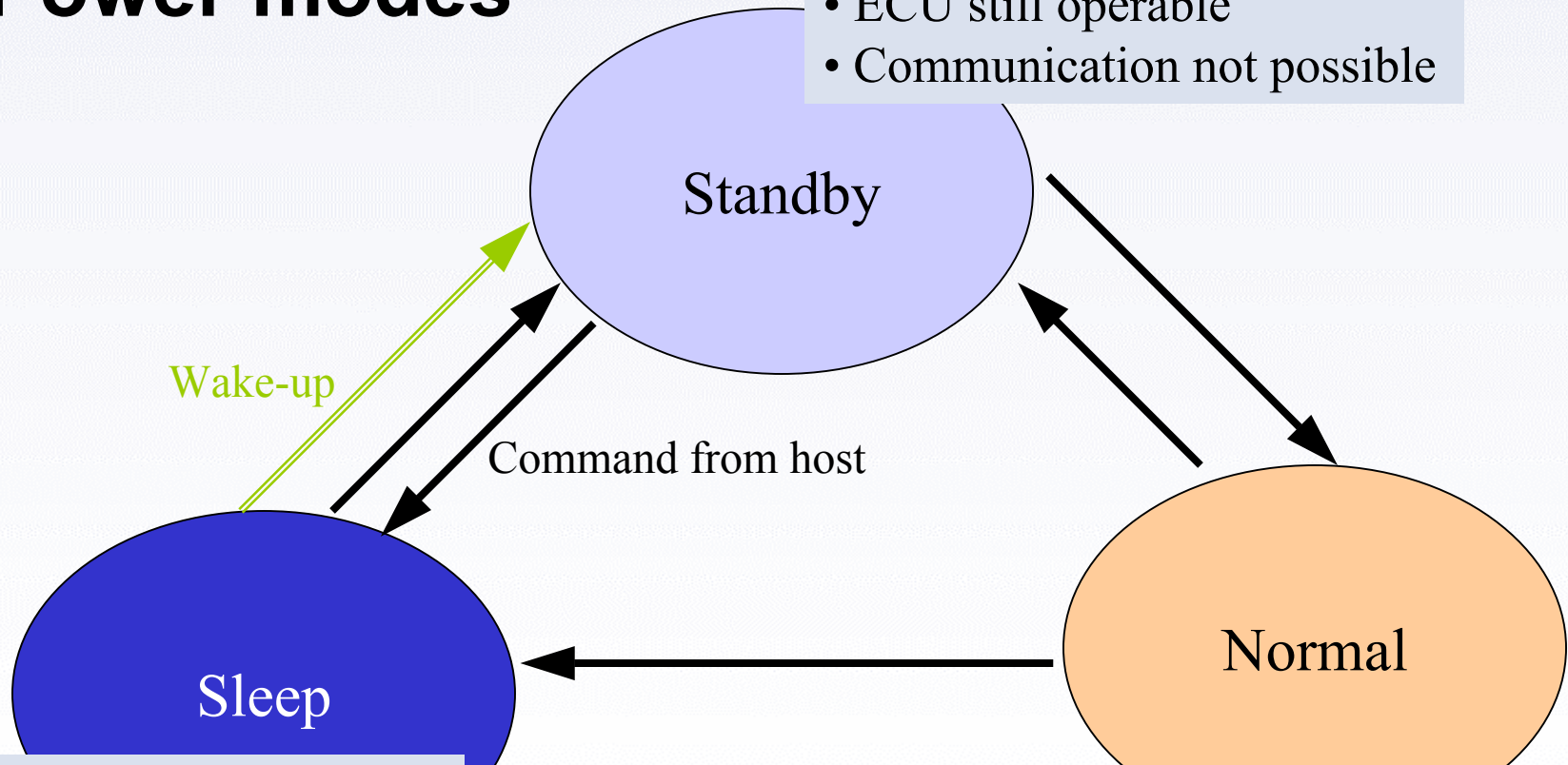


FlexRay - The electrical physical layer

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Power modes

- Reduced power consumption
- ECU still operable
- Communication not possible



- Lowest power consumption
- ECU not operable
- Communication not possible

- Operational power consumption
- ECU fully operable
- Communication possible

Wake up

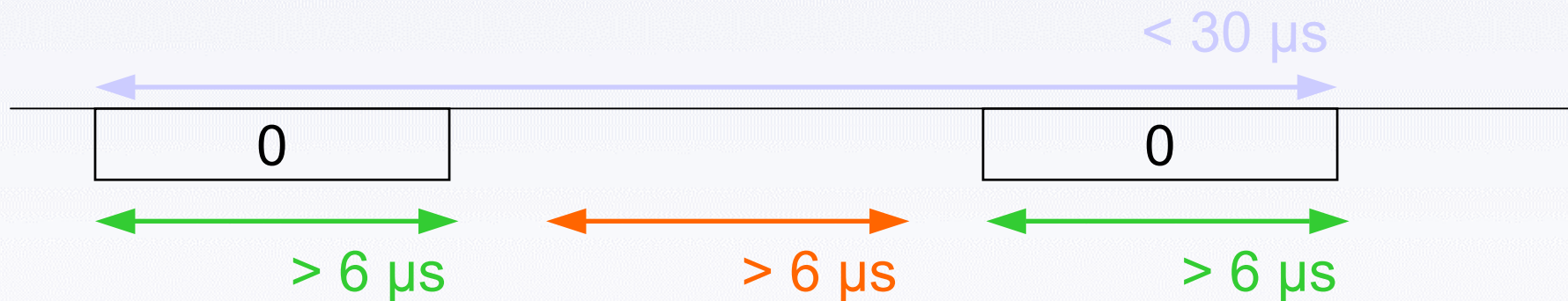
- Requirements of a Wake-Up function
 - Recognition of local initiated wake-up
 - Reliable recognition of remote wake-up via bus lines
 - Low power consumption of wake-up monitoring circuit
 - Robustness against unwanted RF disturbances (EMC)

Wake up

Solutions:

- Local wake-up event
 - Rising or falling edge on wake pin
- Wake-up via bus lines
 - Recognition of special wake-up symbol during start-up
or
 - Receiving a frame with suitable data content

Wake up – special symbol



Wake-Up symbol definition:

Two “dominant_0” phases of at least 6 μs each separated by at least 6 μs idle within a 30 μs interval.

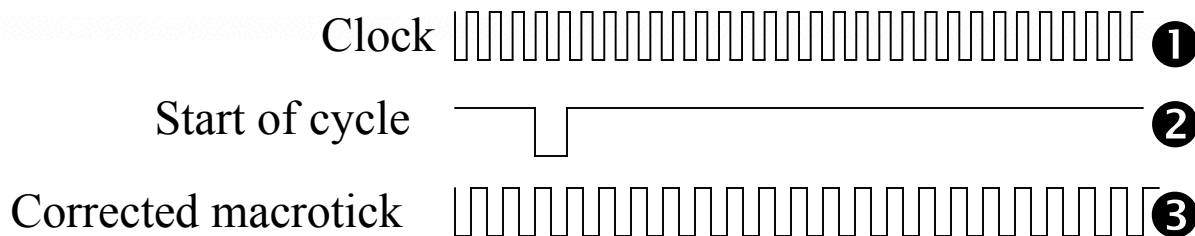
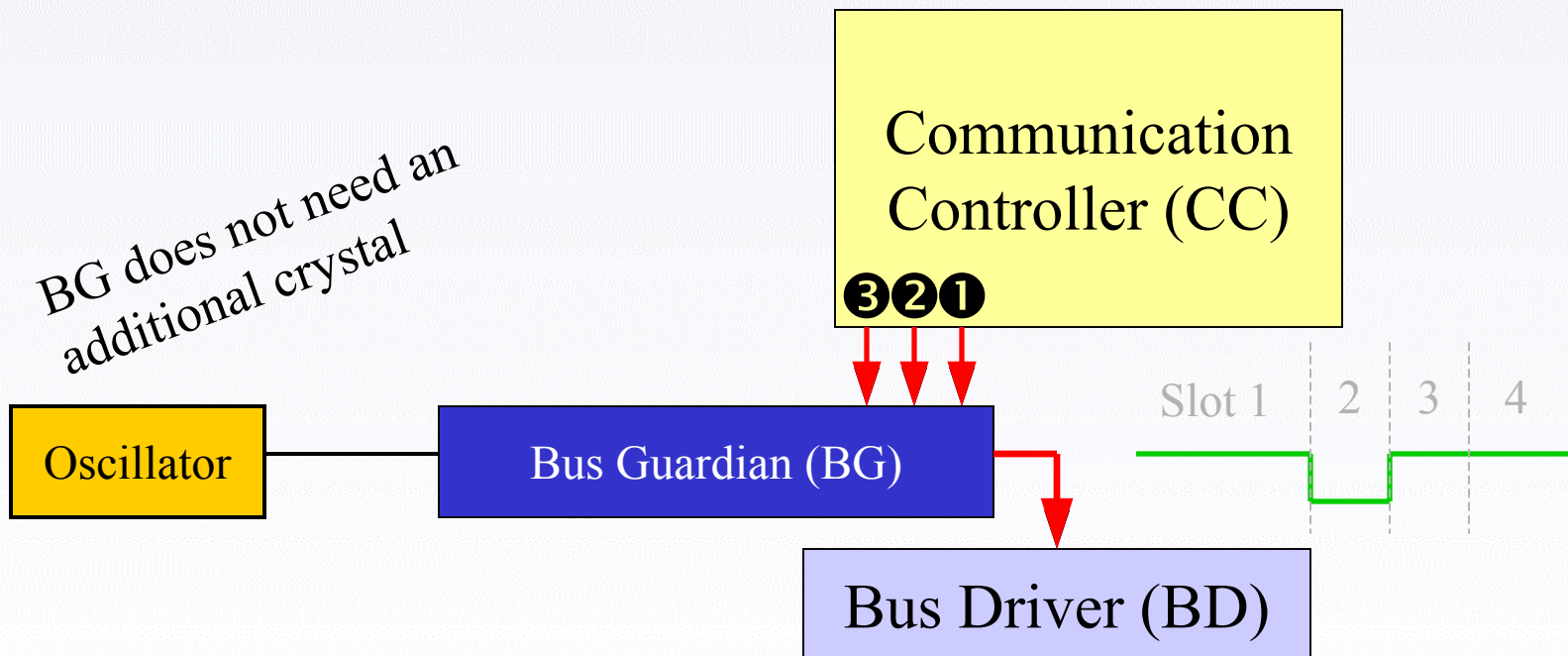
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Bus guardian

- Requirements of a bus guardian:
 - Enable bus driver (prevent babbling idiot)
 - Supervise schedule conformance
 - Supervise clock synchronization

Bus guardian – synchronization



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- **Status of development**
- Outlook to future products

Status of development

- **Philips** bus driver prototype samples and bus guardian FPGAs have been delivered to FlexRay Core Partners in early 2001
 - Laboratory and in-vehicle tests have been made
 - First promising feedback from tests is available

- **Philips** device specifications have been reworked based on field feedback
 - Future production version of bus drivers (transceiver) and bus guardians are under development

Status of development

- Expected availability of hardware components

CC V4.1	CC V6.0	CC V6.x	CC V6.x	CC V6.x
BG FPGA	incompatible	BG FPGA update	BG FPGA update	BD with integrated BG
BD prototype	BD prototype	BD prototype	BD 1 st silicon	BD 1 st silicon
→ Q4/2002	Q1/2003	Q2/2003	Q3/2003	Q4/2003 →

CC: Communication Controller
 BG: Bus Guardian
 BD: Bus Driver

Status of development

- Functional “Electrical Physical Layer Specification V1.1” is available
 - Bus-level-scheme / Electrical characteristics
 - Bus Driver’s basic functionalities
 - Network topology layout possibilities
 - Cable termination concepts
- Functional “Bus Guardian Specification V1.2” is available
 - Bus Guardian’s basic functionalities
- Preliminary [Philips](#) device specifications are expected for Q2/2003

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Outlook to future **Philips** products

- **Bus Driver**

- Main features

- single channel high speed bus driver up to 10 Mbit/s
 - optimized EMC behaviour for FlexRay applications
 - 14 V and 42 V battery voltage compliant



Outlook to future **Philips** products

- **Bus Driver**
- **Bus Driver with integrated Bus Guardian**
 - Main features
 - single channel high speed bus driver up to 10 Mbit/s
 - optimized EMC behaviour for FlexRay applications
 - 14 V and 42 V battery voltage compliant
 - mode control and status information via SPI
 - on-board RC oscillator
(Bus Guardian clock source)

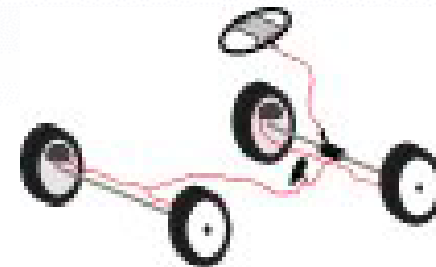
Outlook to future **Philips** products

- **Bus Driver**
- **Bus Driver with integrated Bus Guardian**
- **Active star**
 - Main features
 - autonomous message routing
 - autonomous power moding
 - bus failure containment
 - flexible concept supports a scalable number of single channel branches

Conclusion



is the only high-speed time triggered communication system with a dedicated automotive electrical physical layer solution!





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The communication system for advanced automotive control applications

Thank you for your attention!

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